FIG. 1

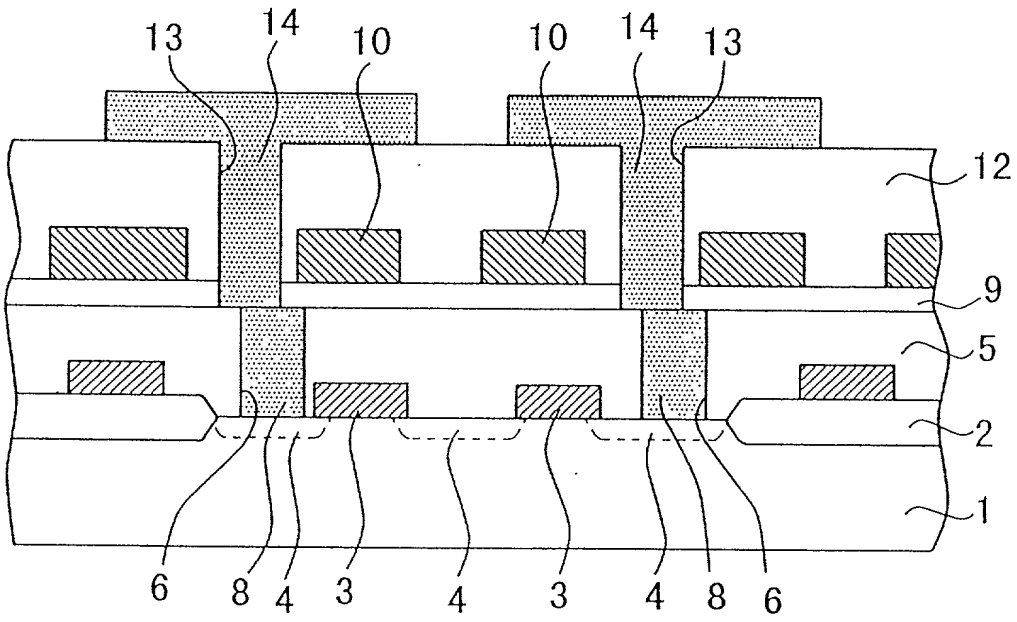

FIG.2

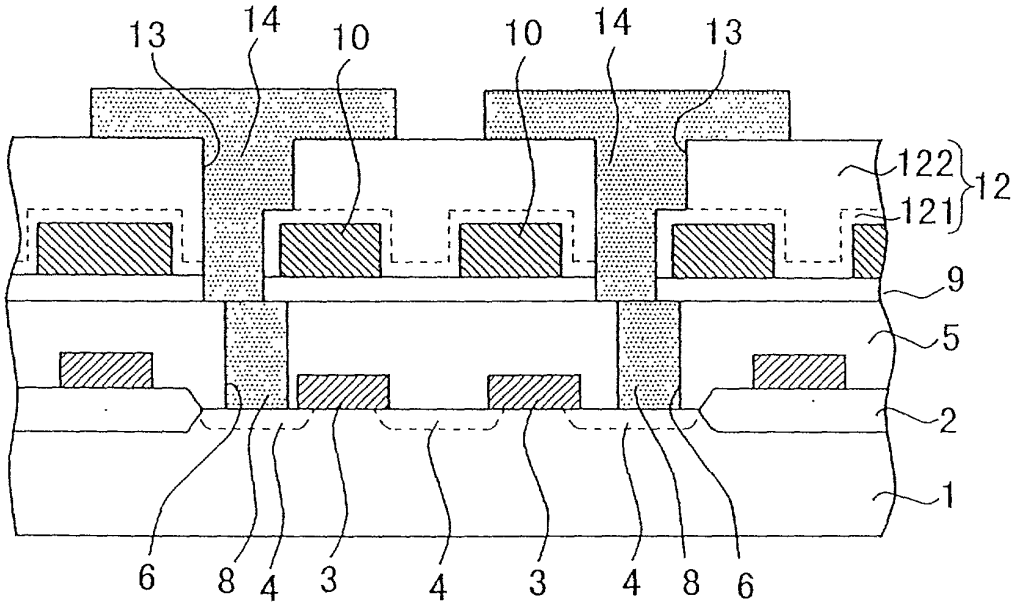

FIG.3

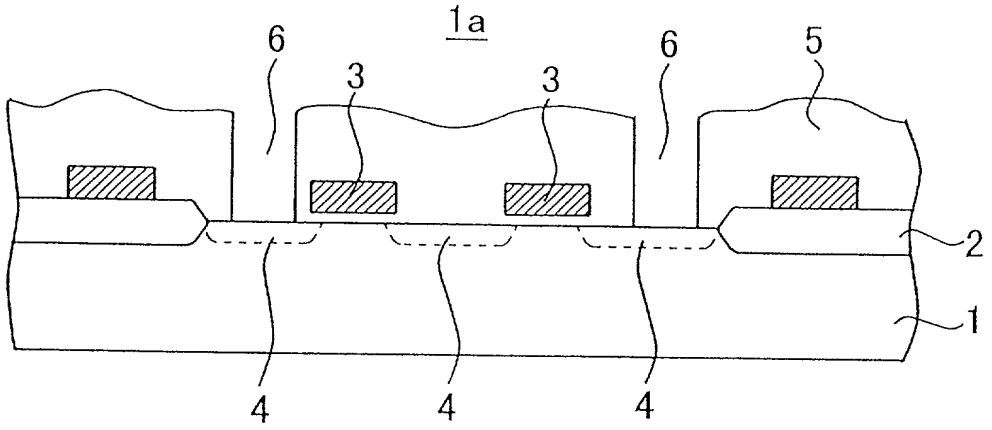

FIG.4

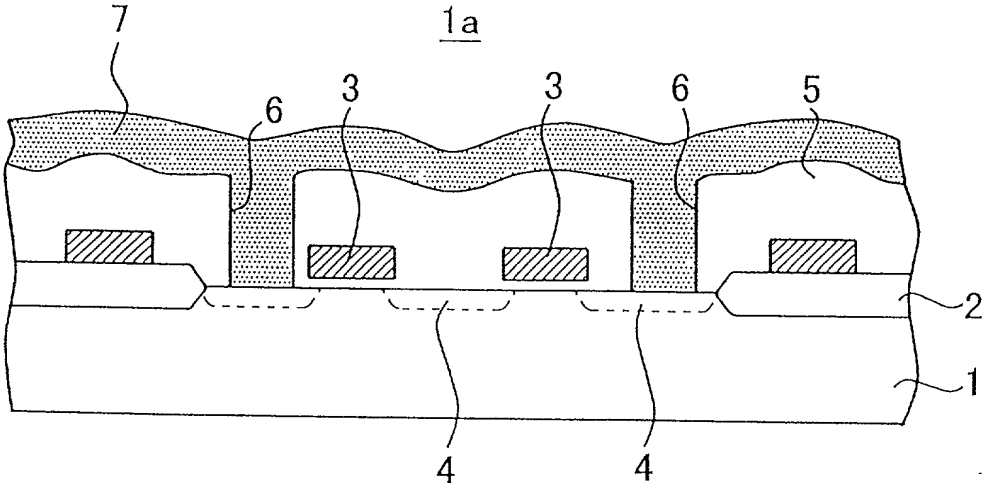

FIG.5

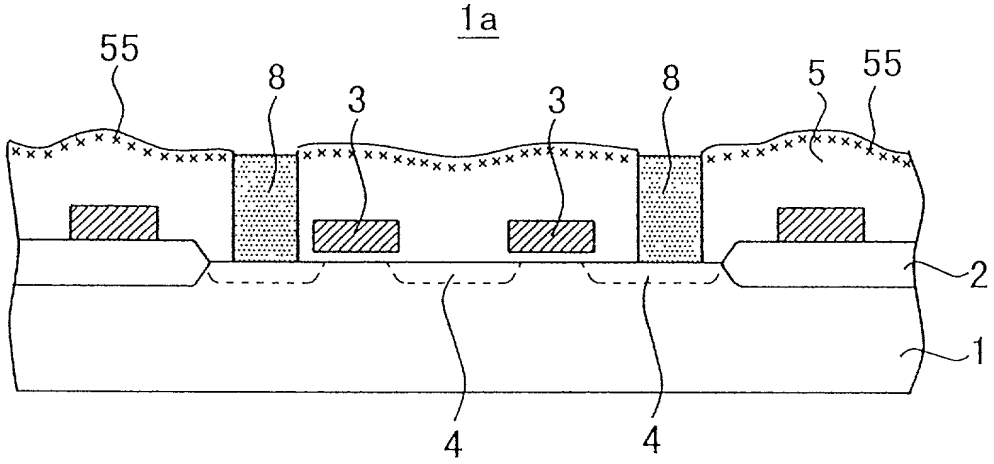

FIG.6

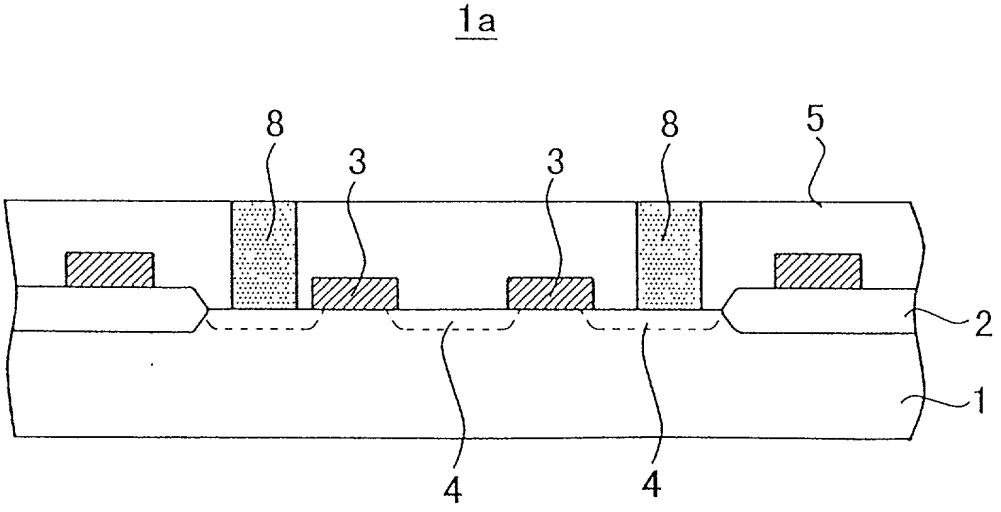

FIG.7

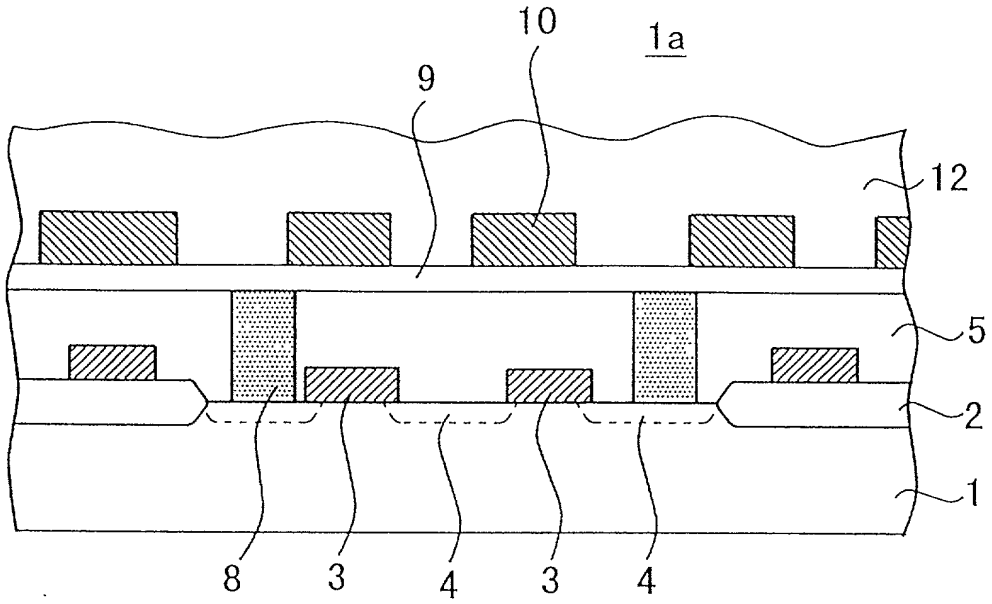

FIG.8

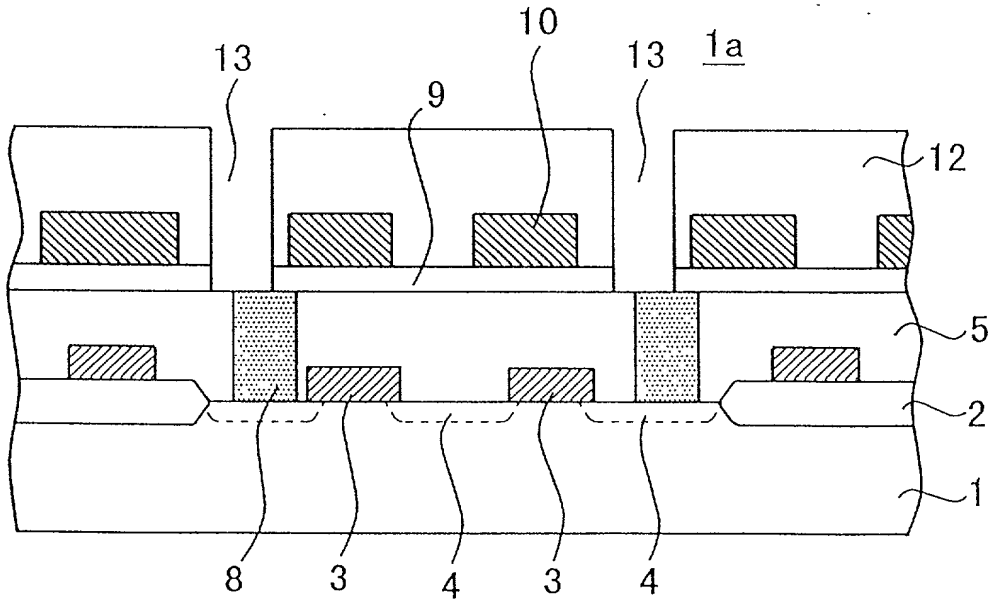

FIG.9

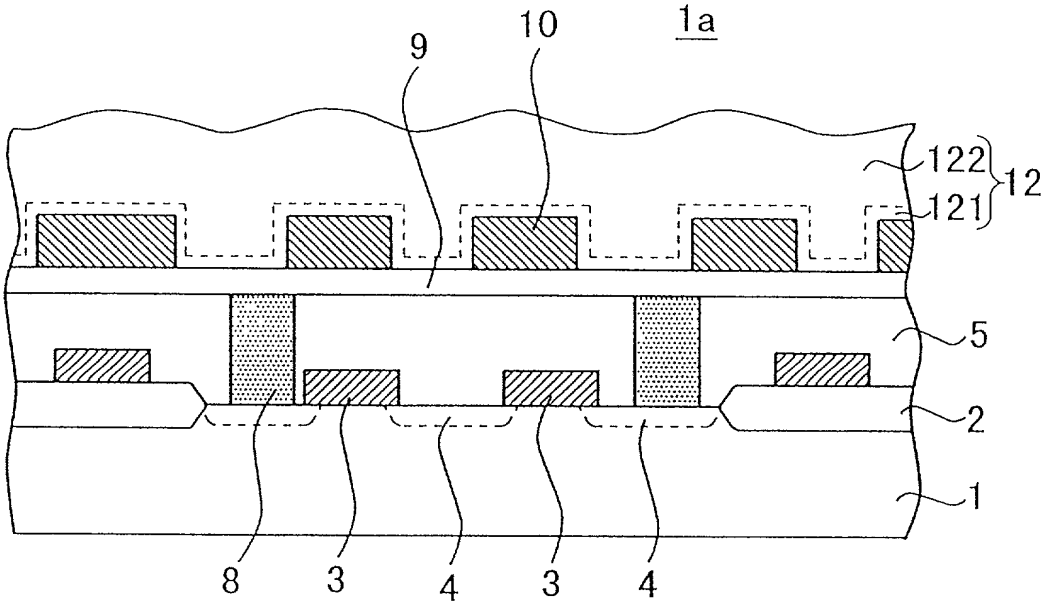

FIG.10

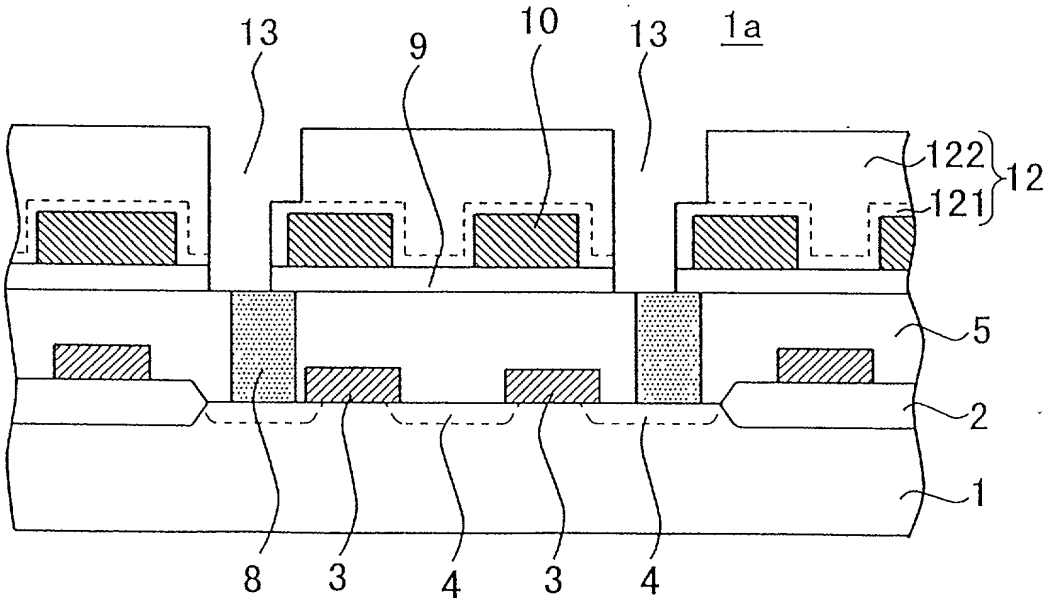

FIG.11

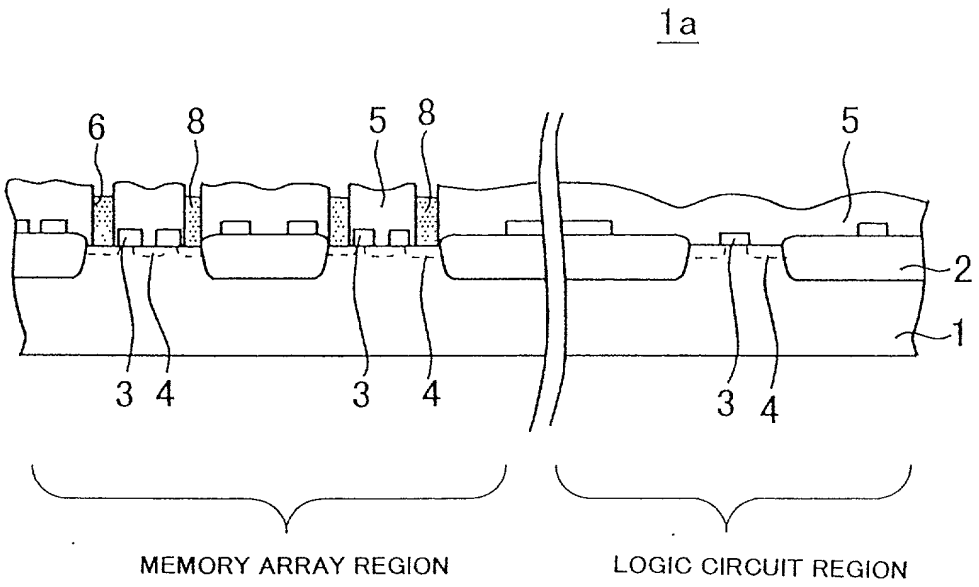
1a
6
8
5
8
5
2
1
3
4
3
4
3
4
MEMORY ARRAY REGION
LOGIC CIRCUIT REGION

FIG.12

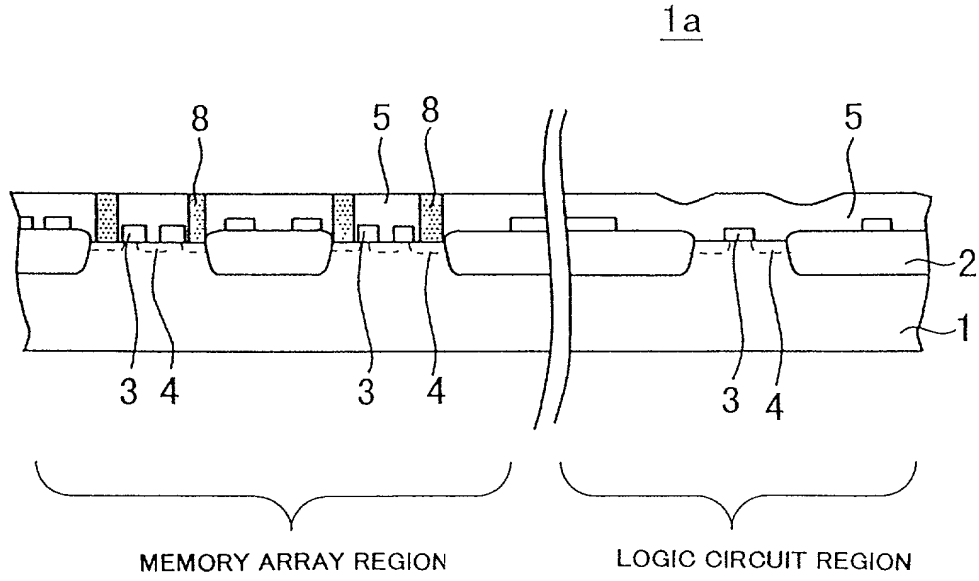
1a
8
5
8
5
2
1
3
4
3
4
3
4
MEMORY ARRAY REGION
LOGIC CIRCUIT REGION

FIG. 14

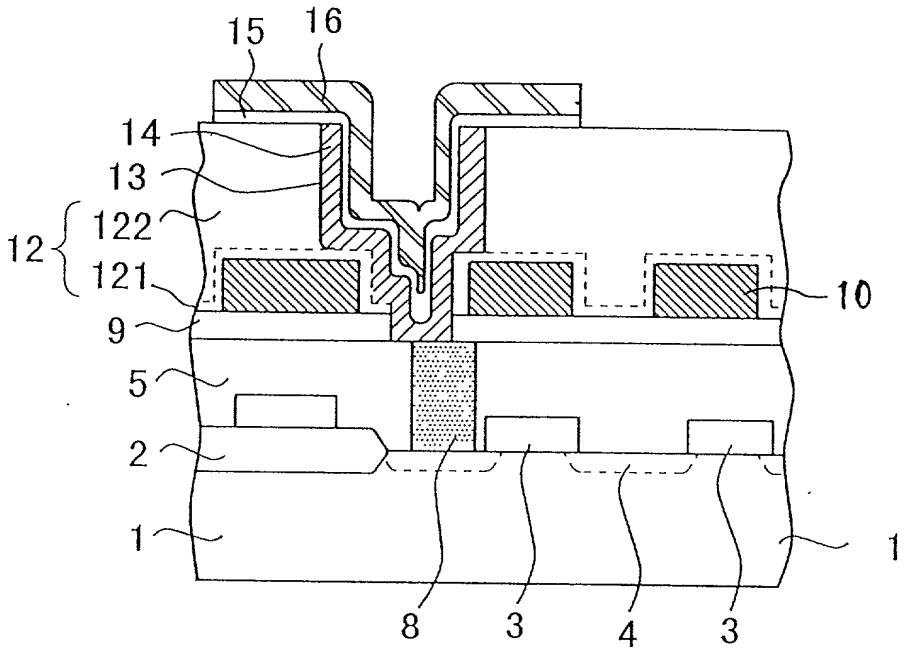

FIG.15

PRIOR ART

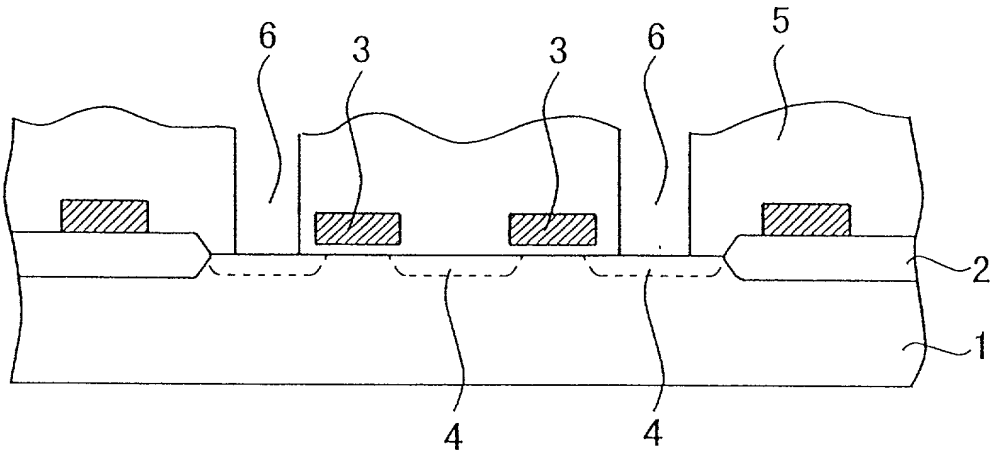

FIG.16

PRIOR ART

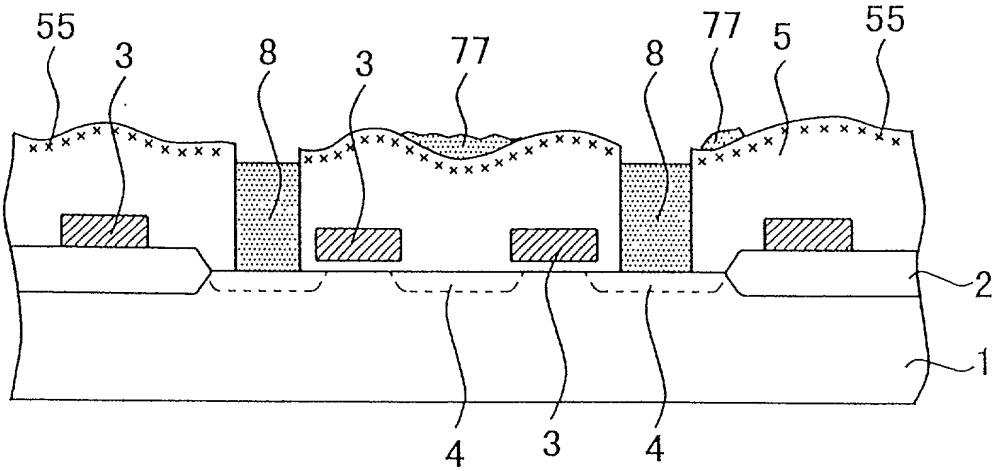

FIG.17

PRIOR ART

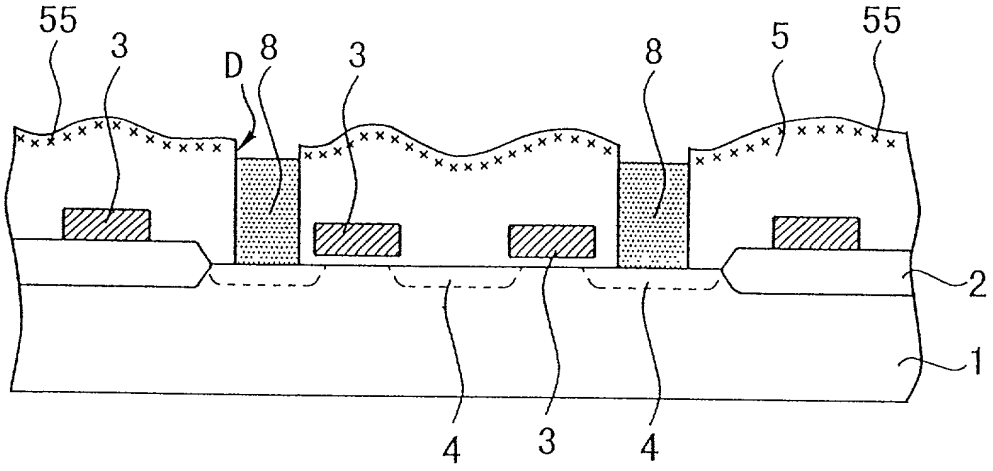

FIG.18

PRIOR ART

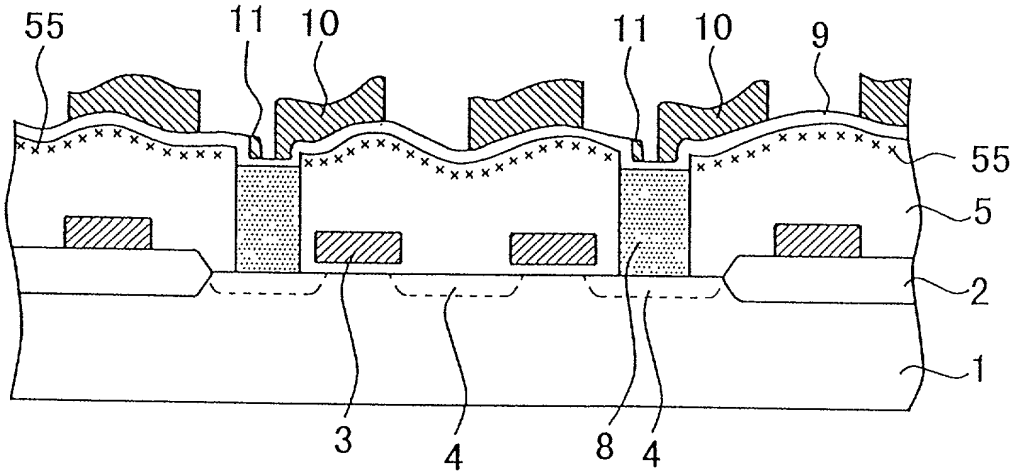

FIG.19

PRIOR ART

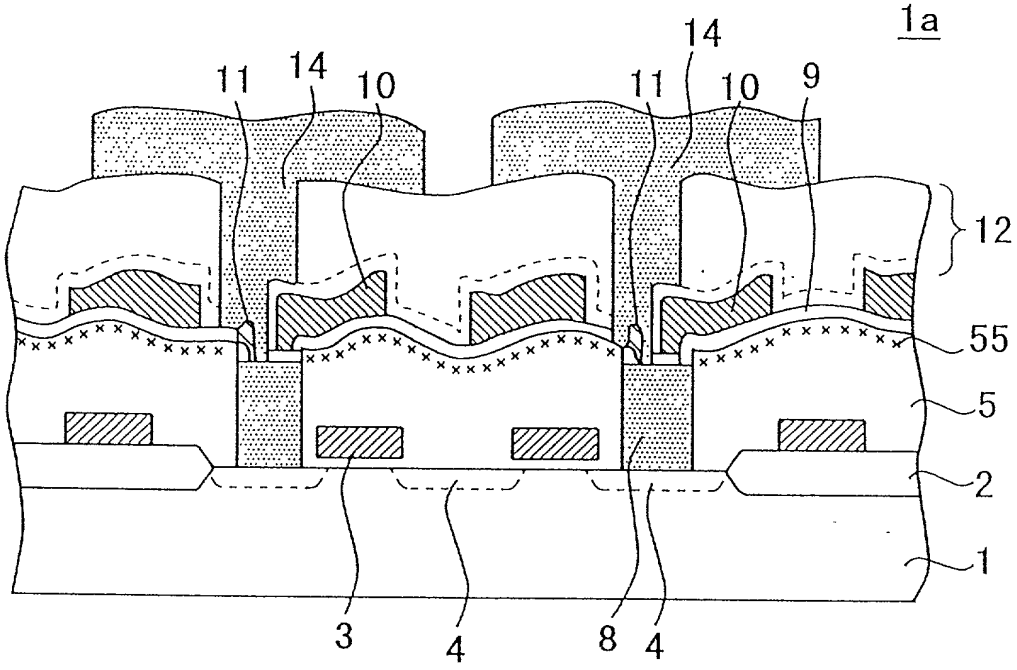

FIG.13

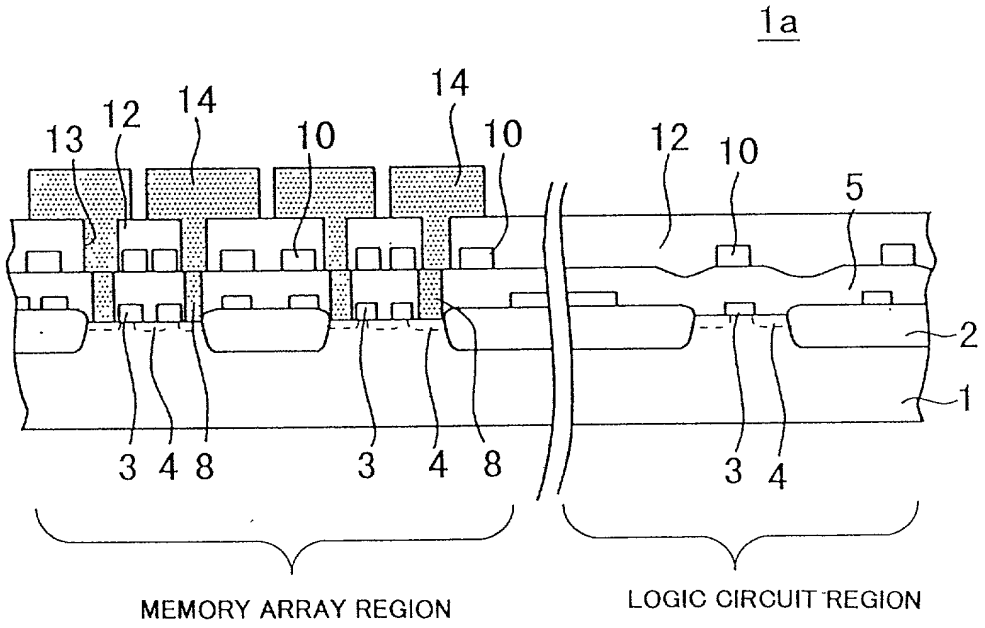
1a
13
12
14
10
14
10
12
10
5
2
1
3
4
8
3
4
8
3
4
MEMORY ARRAY REGION
LOGIC CIRCUIT REGION

FIG.20

PRIOR ART

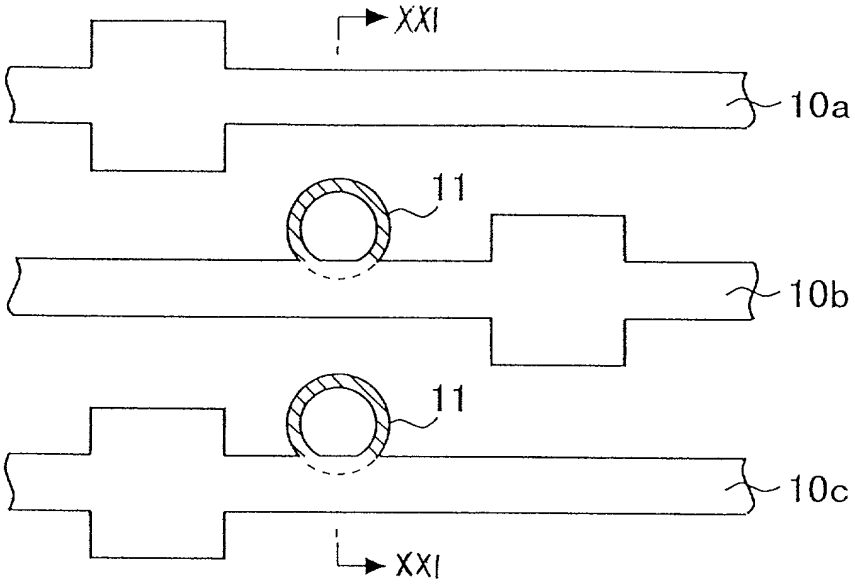

FIG.21

PRIOR ART

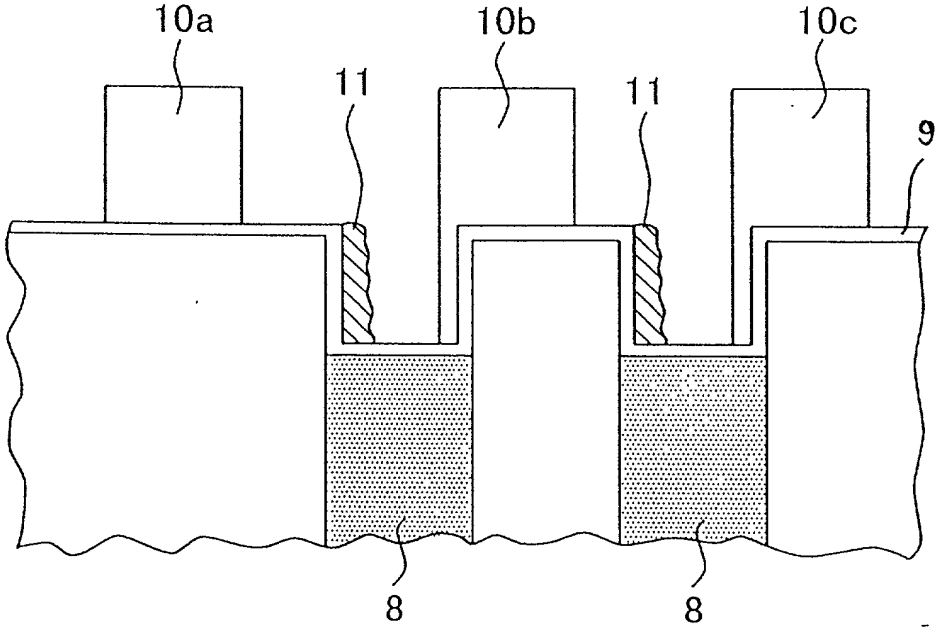

FIG.22

PRIOR ART

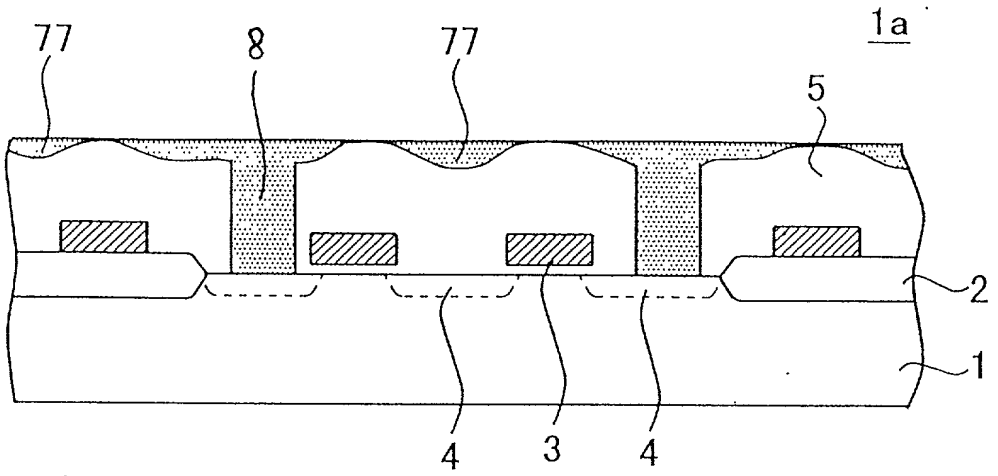

FIG.23

PRIOR ART